HA-5104
SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

Authors: Doug Youngblood and Bobby Huckabee

Introduction

This application note describes the SPICE macro-model for the HA-5104, a low noise quad op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the SPICE net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model simulates most AC and DC parameters. The significant dominant poles and zeros are included to give the most accurate AC simulation with minimum model complexity. The listing is for one of the four amplifiers available on the actual chip.

Model Description

Input Stage

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is created by FA. VIO represents the input offset voltage. C1 is used to limit slew rate. No input parasitics due to package capacitance and lead inductance are included.

Gain Stage

G2, R2, CC, GOL and RD simulate the open loop gain. CC is the compensation capacitor which determines the first dominant pole.

Poles-Zeros

The five poles of the HA-5104 are modeled by RC networks while RL networks are used to model the four zeros. The one complex pole used is modeled by an RCL network. The frequency of all poles and zeros is shown on the macro-model schematic.

Output Stage

EX1, D1, and D2 create output current limiting. IH and IL are the supply currents. FIN and FIP vary the supply currents based on the op amps output current. DL, DH, VL and VH provide voltage clamping on the output to simulate the typical output voltage swing. No output parasitics due to package capacitance and lead inductance are included.

Parameters Not Modeled

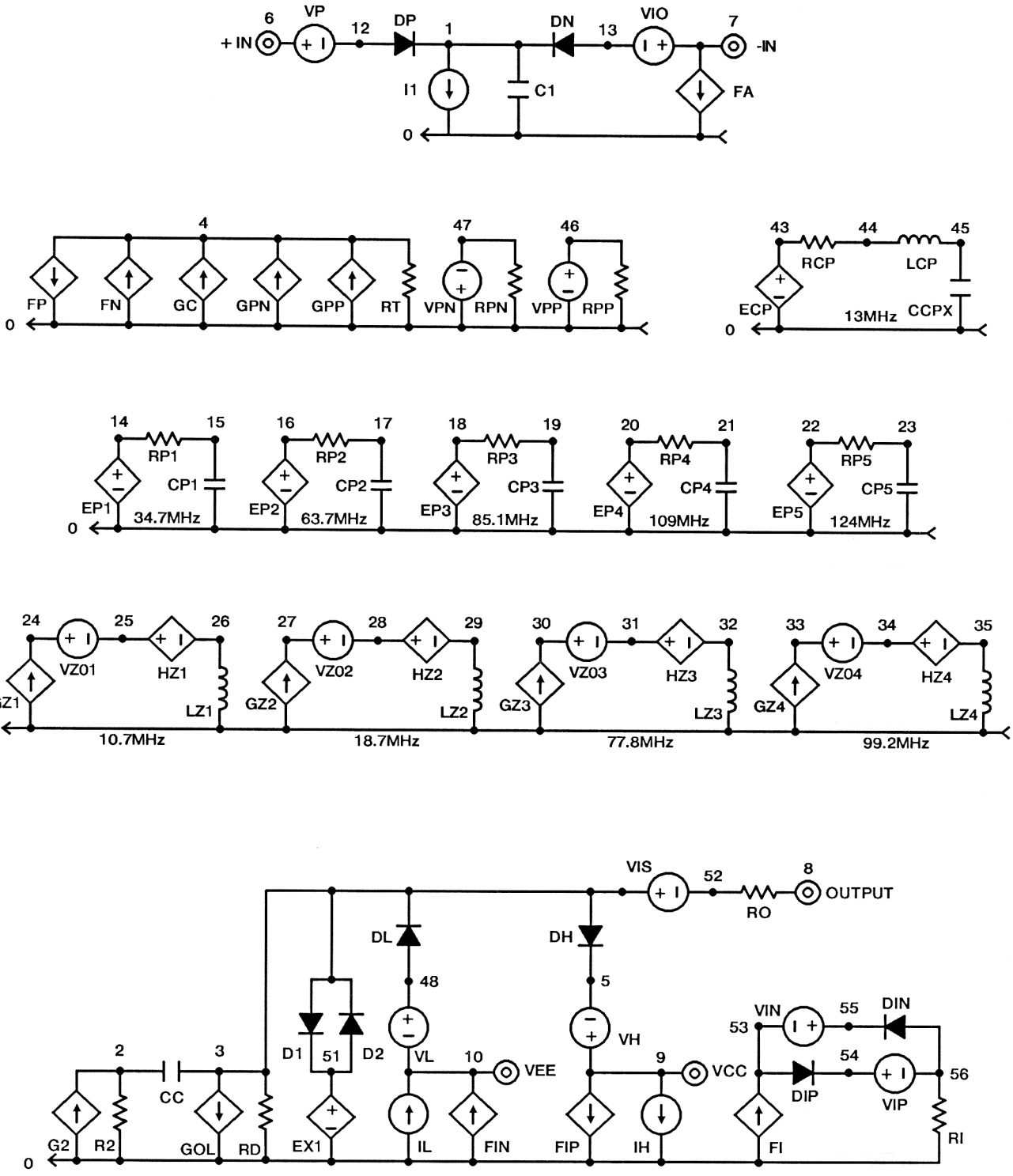
To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Noise Voltage
- Input Noise Current
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

Spice Listing

```
*
* COPYRIGHT © 1991, 2002 INTERSIL AMERICAS INC.
* ALL RIGHTS RESERVED
*
*HA-5104 MACRO-MODEL
*REV: 8/8/91
*BY: D.L. YOUNGBLOOD
*
*THE SCHEMATIC FOR THIS REV. IS THE SAME AS 11/03/89. THE
*SUBCIRCUIT CALL IS DIFFERENT AND ONLY 1 AMP IS PRESENT
*PINOUT CHANGED TO CONFORM TO "STANDARD"
*
*PINOUT:  +IN  -IN  VCC  VEE  VOUT
*
*ACTUAL CHIP ICC/IEE WILL HAVE 4 AMPLIFIERS + 1mA
*
.SUBCKT  HA5104  6  7  9  10  8
.MODEL DP D      IS=1E-14          N=+9.6204E-01
.MODEL DN D      IS=+1.0012E-14    N=+9.6204E-01
.MODEL DV D      IS=1E-14          N=.1
.MODEL D1 D      IS=1E-14          N=1
.MODEL D2 D      IS=1E-14          N=+9.8914E-01
*
*INPUT STAGE
*
VP 6 12 0
DP 12 1 DP
*
*THE VALUE OF SOURCE "VIO" REPRESENTS OFFSET VOLTAGE
*AND MAY BE CHANGED TO SIMULATE WORST CASE IF DESIRED
*
VIO 7 13 +2.2845E-04
*
DN 13 1 DN
FA 7 0 VIO 9.7559E-02
I1 1 0 +5.1342E-08
C1 1 0 +2.6360E-16 IC=-3.6478E-01
FP 4 0 VP   +9.7214E+02
FN 0 4 VIO  +9.7098E+02
GC 0 4 1 0 +1.0090E-08
GPP 0 4 9 46 +9.9726E-10
GPN 0 4 47 10 +1.4492E-08
RT 4 0 1.0
VPP 46 0 +1.5E+01
RPP 46 0 1K
VPN 0 47 +1.5E+01
RPN 0 47 1K
*
*GENERAL POLES
*
EP1 14 0 4 0 1.0
RP1 14 15 +4.5768E+01
CP1 15 0 1.0E-10
EP2 16 0 15 0 1.0
RP2 16 17 +2.4966E+01
CP2 17 0 1.0E-10
EP3 18 0 17 0 1.0
RP3 18 19 +1.8702E+01
CP3 19 0 1.0E-10
EP4 20 0 19 0 1.0
RP4 20 21 +1.4508E+01
CP4 21 0 1.0E-10
EP5 22 0 21 0 1.0
RP5 22 23 +1.2762E+01
CP5 23 0 1.0E-10
*
*GENERAL ZEROS
*
GZ1 0 24 23 0 +1.4852E-02
VZ01 24 25 0.0
HZ1 25 26 VZ01    +6.7333E+01
LZ1 26 0 1.0E-6
GZ2 0 27 24 0 +8.5174E-03
VZ02 27 28 0.0
HZ2 28 29 VZ02    +1.1741E+02
LZ2 29 0 1.0E-6
GZ3 0 30 27 0 +2.0450E-03
VZ03 30 31 0.0
HZ3 31 32 VZ03    +4.8900E+02
LZ3 32 0 1.0E-6
GZ4 0 33 30 0 +1.6037E-03
VZ04 33 34 0.0
HZ4 34 35 VZ04    +6.2354E+02
LZ4 35 0 1.0E-6
*
*COMPLEX POLE
*
ECP 43 0 33 0 1.0
RCP 43 44 +2.4045E+04
LCP 44 45 +1.4988E-04
CCPX 45 0 1.0E-12
*
*GAIN/OUTPUT STAGE
*
G2 0 2 45 0 1.0
R2 2 0 +8.9835E+05
CC 2 3 +2.2000E-11
GOL 3 0 2 0 +6.1330E+01
RD 3 0 +4.6980E+00
DH 3 5 DV
DL 48 3 DV
VH 9 5 1.607
VL 48 10          1.5986
IH 9 0 +1.0E-03
IL 0 10 +1.0E-03
D1 3 51 D1
D2 51 3 D2
EX1 51 0 POLY  2  3  0  3  8  0  1  -4.0840E-01
RO 52 8 +1.0611E+02
VIS 3 52 0
FI 0 53 VIS 1
DIP 53 54 DV
DIN 56 55 DV
VIP 54 56 0
VIN 55 53 0
RI 56 0 1.0
FIP 9 0 VIP 1.0
FIN 0 10 VIN 1.0
.ENDS HA5104
```

Macro-Model Schematic

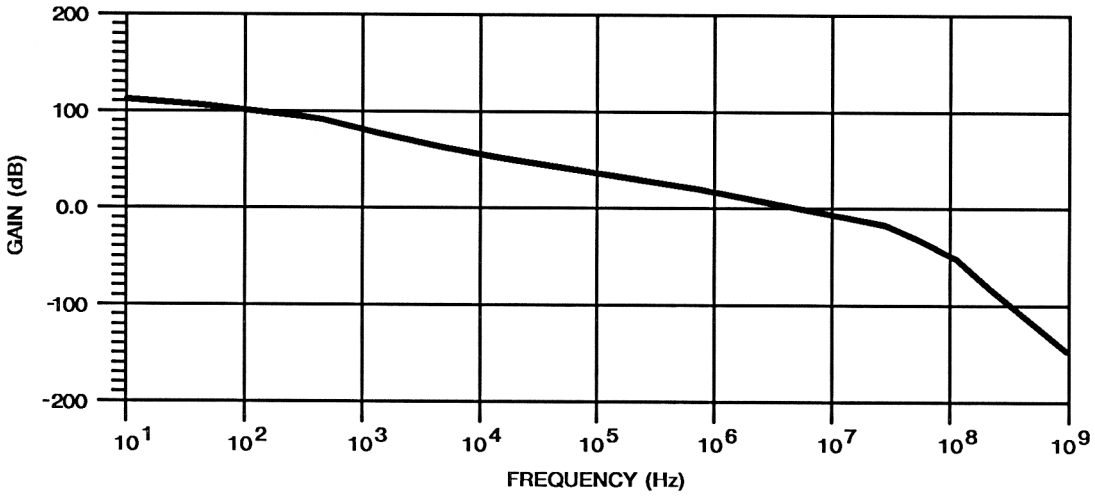


All Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

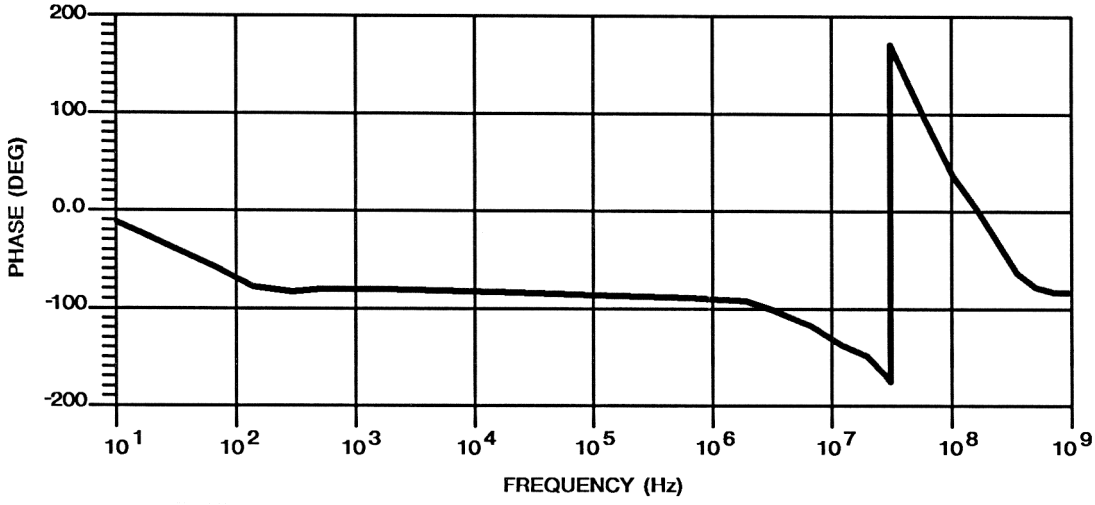
Model Performance

Conditions: V_{SS} = ±15V, A_{VCL} = +1, Unless Otherwise Specified

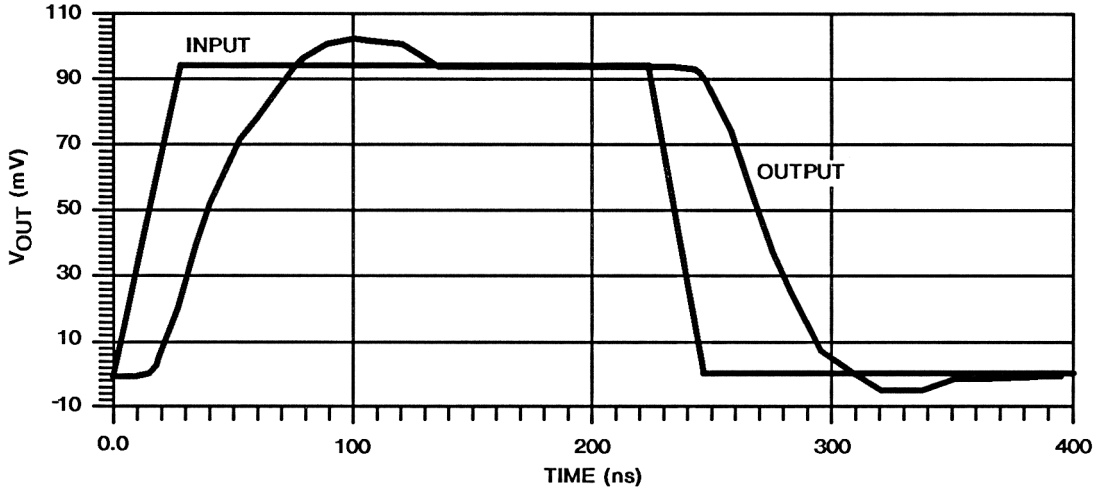
OPEN LOOP GAIN PLOT
(R_L = 2K, C_L = 50pF)



OPEN LOOP PHASE PLOT

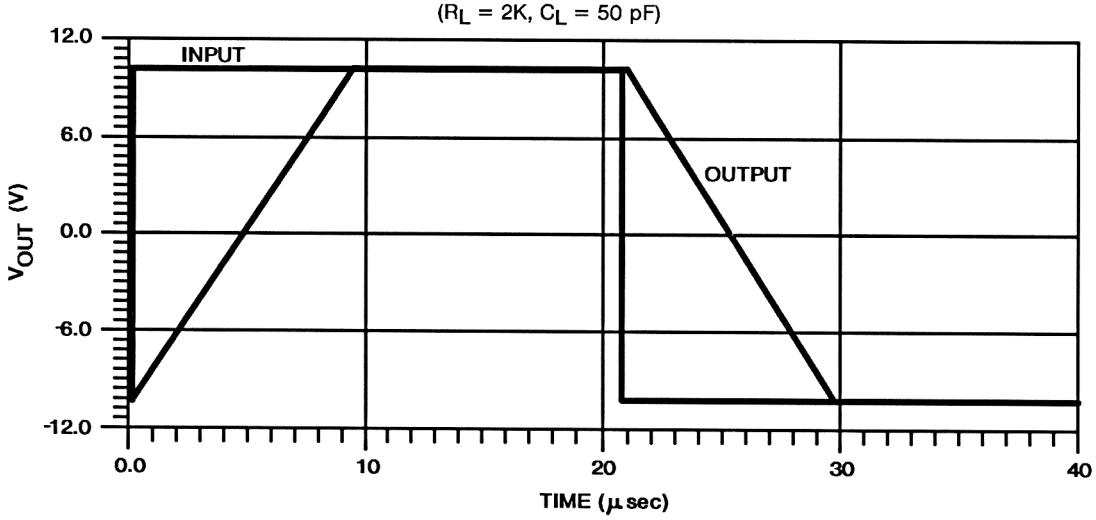


SMALL SIGNAL RESPONSE
(R_L = 2K, C_L = 50pF)

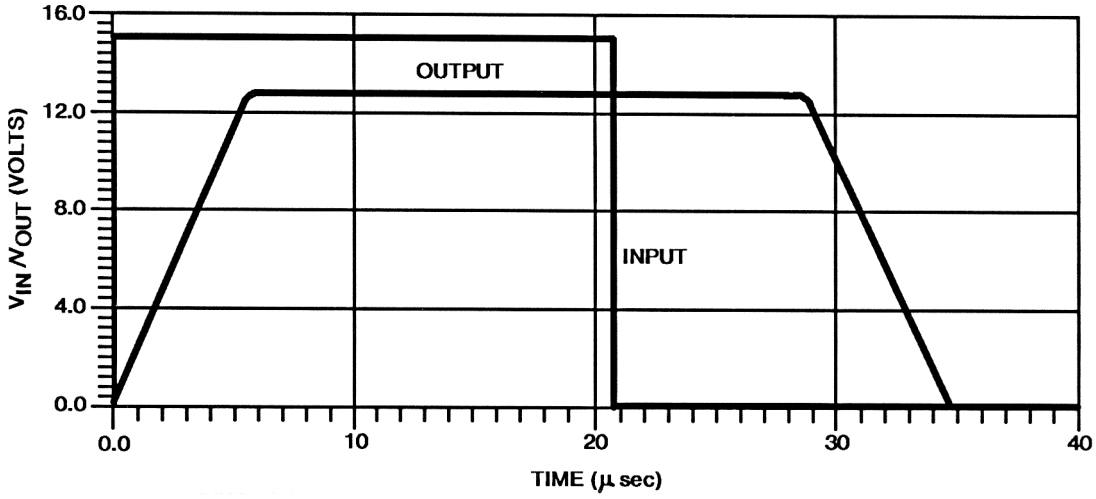


Model Performance (Continued)

LARGE SIGNAL RESPONNSE
(R_L = 2K, C_L = 50 pF)



MAXIMUM POSITIVE OUTPUT SWING AND SATURATION DELAY



MAXIMUM NEGATIVE OUTPUT SWING AND SATURATION DELAY